

ALTHOUGH DEVICE AND PARASITIC EXTRACTION HAS BEEN AN ISSUE AT EACH TECHNOLOGY PROCESS NODE, AT 130 AND 90 NM, IT HAS BECOME THE MAJOR ISSUE. TODAY, SIMULATION MAY NOT ACCURATELY ACCOUNT FOR AN ANALOG DEVICE'S UNIQUELY SHAPED DIFFUSION AND MAY CREATE A STRESS THAT MAY CAUSE AN ENTIRE CHIP TO FAIL.

Getting to silicon: accuracy requirements of nanometer designs

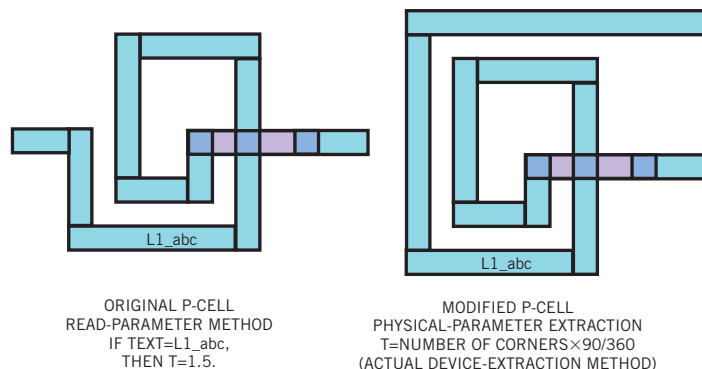
DEVICE AND PARASITIC extraction has always been an issue at some level. Analog designs are handcrafted and are more prone to signal flaws than are digital designs. Therefore, they have a greater impact on full-chip power and electrical behavior. At larger process technologies, such as 250 nm, engineers could handle device extraction with an LVS (layout-versus-schematics) tool using an assumptive method of measuring physical parameters. They could also perform parasitic extraction by using tools employing simple cell characterization at the gate level. However, in the nanometer era, with its advanced functions, complicated interconnect, mixed-signal components, and restricted on-chip real estate, assumptive parameter measurement, and gate-level extraction become insufficient. Designers need more extensive data to perform accurate simulation and to solve the ever-increasing parasitic effects that can cause chip failures, such as noise, faulty timing, and reduced power and signal integrity.

NEVER ASSUME

It is now harder than ever to ensure that simulations match the intent of the chip. At nanometer processes, accurate simulations require data from the actual physical geometries. Unfortunately, most LVS tools do not handle device parameters in this way. Instead, they rely on Pcell (parameterized-cell) assumptions. These types of LVS tools look for a device or an element in the layout, labeled "XYZ," for example, that matches that device or element with those in the schematic named XYZ and assume that all have identical parameters. With digital designs, typically developed in standard repetitive format, such device assumptions can be acceptable.

In digital designs, it is often easier for the LVS tool to extract simple physical parameters, such as the length and the width of transistors.

It's a different matter when measuring parameters of unique analog or other nonstandard devices. A layout designer may flatten or change an instance for the device labeled XYZ. Using the Pcell method to generate the device extraction means that the flattened and changed device still compares correctly with an XYZ device in the schematic, even though its parameters may differ greatly from the contents of the schematic and the simulation used. A modified device in the layout substantially impacts chip behavior. Common situations illustrate this problem: unique inductors, unique diffusion, and non-standard transistor layout.



CASE	OPEN LOOP	ACTUAL DEVICE
ORIGINAL	T=1.5	T=1.5
MODIFIED	T=1.5	T=1.75

Figure 1

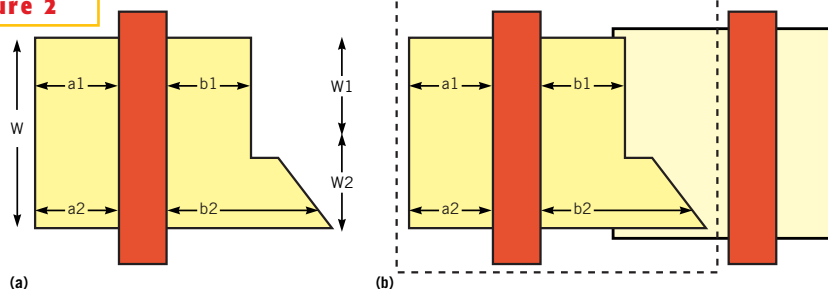
A minor change to a crucial component can cause a significant shift in the desired performance of a design.

Most LVS tools assume that an inductor in the layout identified in a naming convention has parameters that match those in the schematic. But if the designer has modified the Pcell, adding coils or turns, it not only changes the device parameters, but also affects the performance on the chip. **Figure 1** shows that, there are 1.5 turns in the original Pcell for inductor L_{1-abc} . In the modified case, the layout designer has flattened the Pcell and added a short line to bring both terminals onto the same side of the inductor. This approach effectively adds another quarter-turn to the inductor, potentially increasing the actual inductance by as much as 16%. Changing this parameter without also modifying the Pcells results in inaccurate simulation. Manufacturing a chip with inaccurate simulations more than likely will result in costly respins. According to recent statistics, an average of 2.6 spins are necessary to achieve a working analog-mixed-signal design in silicon.

An LVS tool that relies on Pcell methodology for comparison does not guarantee a correct comparison of the physical layout device to the schematic. This method of device extraction and comparison is not a true verification because it compares the model parameters with themselves. The only way to determine that the physical layout is equivalent to the model is to extract and measure the physical parameters in the layout. You can then compare these physical parameters with the parameters in the model to ensure that the built circuit is indeed equivalent to the simulated circuit and vice versa. The main reason to employ Pcell comparison is that it is difficult, if not impossible, for most LVS tools to properly extract the physical parameters. However, for relevant simulation, the designer should know not only the basic parameters, such as the length and width of transistors and other devices, but also the unique or difficult-to-measure parameters necessary for accurate simulations.

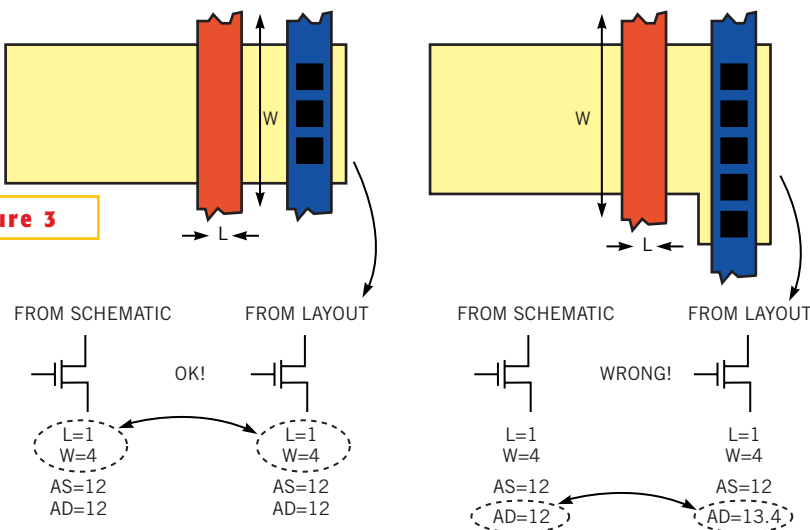
The diffusion area of a MOS device illustrates the need to consider these additional parameters. Simulation of diffusion gives designers an accurate picture of power and reliability—how long the device will perform before it “stresses.” Engineers design most diffusion areas with simple straight lines—typically, a rectangle. However, designers may create irregularly shaped diffusion areas to accom-

Figure 2



Simulation does not accurately recognize irregularly shaped diffusion unless you take an exact measurement of all physical parameters (a). At a higher level of the hierarchy, a layout designer can overlap existing diffusion with new diffusion from the parent cell (b).

Figure 3



Nonstandard transistor layouts require an LVS tool that extracts actual device parameters—the only way to ensure accurate simulation.

modate neighboring devices in a dense layout (**Figure 2**). This practice is common in analog design; however, uniquely shaped diffusion can interfere with the free flow of current. If you do not detect or measure it, it can cause chip failure.

The only way to determine in simulation that uniquely shaped diffusion is interrupting current is by accurately measuring the physical parameters and feeding the data to the simulator. An LVS tool that relies on parameterized cell data to determine measurement of diffusion wrongly assumes the data for nonstandard diffusion. Without extracting the physical measurement, a true verification cannot take place. Changes in diffusion occur frequently. Designers can place a Pcell when creating lower level hierarchy cells. Later, at a higher level of the hierarchy, a layout designer may overlap the diffusion with new diffusion he drew

from the parent cell. This method not only saves space on the chip, but also creates undesirable results that go unnoticed during simulations, causing a chip to fail.

Engineers must also account for nonstandard transistor layouts in LVS-device extraction. Traditional LVS methods copy parameter information from the schematic rather than compute it directly from the layout. However, if a transistor layout deviates from standard and the tool does not accurately measure the deviation, it cannot support “from-layout” device parameters, as in a MOSFET (**Figure 3**). Accurate simulation requires comprehensive data that comes from an LVS tool that recognizes standard naming devices and then goes deeper, measuring the device turns, wire space, core area, width, length, and other parameters until it has mined all physical-parameter data. Until that point, the tool cannot

correctly compare these parameters with those in the models.

NANOMETER-ERA PARASITIC EXTRACTION

Nowadays, designers must account for a laundry list of new physical effects. Since the 130-nm node and the upswing in first-silicon failures, a large spectrum of new capacitance and resistance interactions have become relevant. Vias are now significant contributors to net parasitic capacitance (Figure 4). Smaller geometries allow for higher operating frequencies, making interconnection inductance relevant. Copper interconnects to reduce parasitic resistance are harder to control dimensionally and cause interconnect-resistance variations across a die. They also require greater metal uniformity to control these variations, which means designers must insert metal fill, also affecting circuit performance.

All of these issues point to the need for more extensive parasitic extraction data as input to simulation and analysis. As a result, designers must obtain evidence of unintentional parasitic effects at the transistor level. That level of detail may include static timing for traditional timing analysis and overall net delay, dynamic timing for propagation delay with all circuitry active, noise for crosstalk and signal-integrity issues, power for IR drop and hot spots, and reliability for yield analysis and electromigration.

The way designers model transistors has also changed. Parameters that were once part of transistor models, such as diffusion resistances, polysilicon-gate resistances, and polysilicon-to-contact capacitances, are now becoming part of the parasitic network. Level 9 of the BSIM3 (Berkeley Short-Channel IGFET Model 3) has made way for Level 14 of the BSIM4, which includes new effects. These effects are gate resistance, gate resistance as a function of sheet resistance and the number of gate contacts, substrate resistance, an added five-resistor network, overlap capacitance, and layout-dependent parasitics.

However, the new effects in the BSIM4 model do not accurately model diffusion resistances, polysilicon-gate resistances, and polysilicon-to-contact capacitances effects. Number squares are too crude, and spacing applies only to single contacts. Accurate simulation requires actual device-parameter extraction. Users can

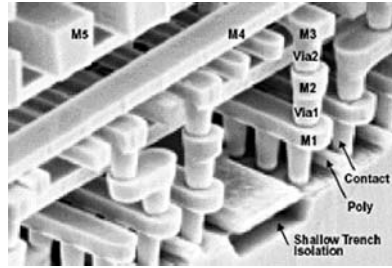


Figure 4 A copper-process cross-section may include vias, conformal dielectric layers, copper wiring, and nonrectangular cross-sections that produce complex interactions. Engineers need to correctly model these parameters to determine parasitic effects (courtesy TSMC).

decide what to put in and what to extract from the device model (Figure 5). In the example, designers can remove the polysilicon-gate resistance from the device model and extract it up to one-third the way into the polysilicon-gate area using the parasitic-extraction tool. This method allows them to then extract the proper values for via resistances and capacitances, regular polysilicon, and gate polysilicon.

To gain accurate simulation and put the results to good use, designers must be able to integrate parasitic information into their design environment. They must be able to integrate postlayout information as a circuit or a subcircuit suitable for simulation. For this situation to occur, designers need accurate extraction

of intentional devices; physically measured parameters; and the ability to properly back-annotate devices, gates, and nets from the layout with the original design source.

Enabling this function requires a tight integration between the LVS and parasitic-extraction tools. Proper back-annotation for simulation in any of the multiple transistor-level flows requires a connection to an LVS tool that enables multiple parasitic-extraction flows. The tools need to provide accurate intentional device recognition for the variety of devices, including transistors, inductors, capacitors, and varactors, that today's analog-mixed-signal designs implement. Tight integration among the design environment, LVS tool, parasitic-extraction tool, and analysis tool ensures efficient data handling for both design-creation environments and postlayout analysis. Using a hierarchical LVS tool with a transistor-level parasitic-extraction tool offers the designer the essential ingredients for accurate nanometer-silicon modeling.

RECOMMENDED FLOW FOR ACCURACY

Designers can avoid the resource drain and technical shortcomings of a multiple-tool environment by streamlining the design flow with a robust tool suite that has a tightly integrated parasitic-extraction and LVS tool at its core. An extraction tool flow provides the best approach to providing accurate data of parasitic el-

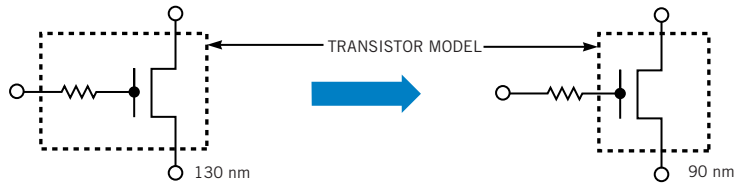
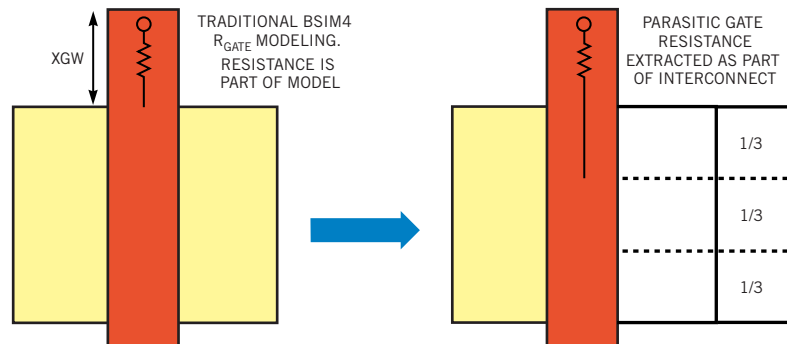


Figure 5



Designers can use a robust parasitic-extraction tool to compensate for BSIM4 inaccuracies.

ements in SOC (system-on-chip) designs. Most important, a streamlined single flow yields a consistent, confident design. It also offers advanced data management to handle the many parasitic elements that designers must extract from SOC designs. The key is to choose tools that do not assume data but account for the physical effects that occur in nanometer designs. Such a tool suite provides the highest accuracy for postlayout simulation. When choosing a tool set, consider the following attributes. It should provide a single set of common intentional device models that LVS and parasitic-extraction tools share. It should also offer actual device-parameter recognition, parasitic extraction at both the transistor and the gate levels, compensation for inadequate BSIM4 modeling, back-

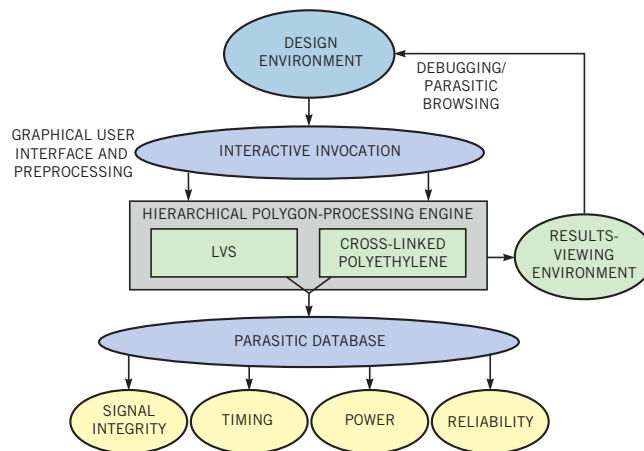


Figure 6

A tight link between LVS and parasitic-extraction tools enables back-annotation to the source layout. In the Calibre design flow, the tool stores extracted parasitic values in a database for on-call, mixed-level analysis.

annotation of simulation results to the source schematic, and seamless integration into various analysis and simulation procedures. The tool suite should also provide design-style independence to handle the various components of SOC

designs and offer strong foundry support for downloading rule files. Tools with these recommended flow characteristics are now available, providing designers with the highest levels of data accuracy for postlayout simulation (**Figure 6**). □

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