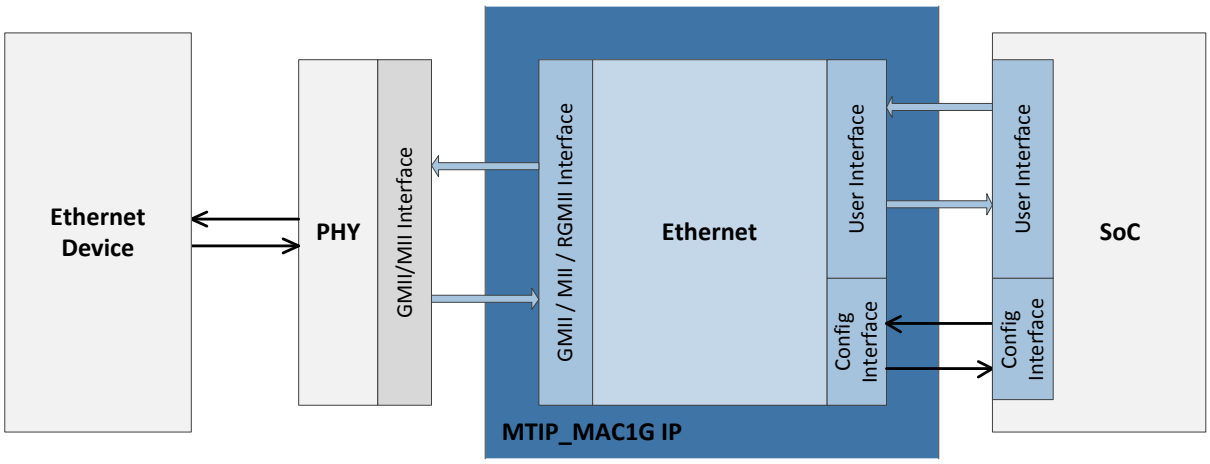
DO254-IP: ETHERNET®

KEY FEATURES

- Developed according to RTCA/DO-254 ED-80 guidance. Compliant DAL A
- Compliant with IEEE Std 802.3-2002 Ethernet Edition, IEEE 802.1Q-1998 Edition, UNH Certified.
- Simple FIFO User Interface.
- Compliant with GMII / MII IEEE Std 802.3, RFC2665, RFC2863 and RFC2819 (www.ietf.org)
- MoreThanIP intellectual property (www.morethanip.com)



TECHNICAL FEATURES

- Tri-Mode 10/100/1000 Fully integrated Ethernet MAC in Full-duplex.
- Supports Preamble, SFD and frame padding generation, CRC on both Rx and Tx path.
- Support for VLAN tagged frames according to IEEE 802.1Q and 9kB jumbo frame.
- Configurable to support 10Mbps, 100Mbps or 1Gbps operation.
- 32 bits simple FIFO interface to user application compatible with simple FIFO interface.
- User interface for Configuration Registers and status information (VLAN tag, frame type and errors).
- GMII (125MHz) or MII (25MHz) interface to Ethernet PHY device.
- Full report done to remote peer and to SoC. (Parity on data buffers, FSM monitoring).
- CRC-32 with optional forwarding of the FCS field.
- Autonomous and dynamically configurable XON/XOFF Pause Frame (802.3 Annex 31A) support.
- Optimized for low gate count (20k-40k gates) and low core latency. Technology independent (Altera/Xilinx/Actel/ASIC).
- Configurable buffer size from 64B to 16kB depending on performance requirement.
- Optional support of AMD Magic Packet detection for node remote power management.
- Support multiple MAC address filtering and multicast address filtering on Rx path with hash table.

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OVERVIEW

The MTIP_MAC1G module provides, with a single IP Core, a solution for Ethernet applications operating at 10/100 or 1Gbit. It allows a SoC to be connected to an external Ethernet Network. The hardware item only covers digital layers of the IEEE 802.3 MAC bus architecture. It supports transparent (for switching application) and full Ethernet frame handling for connected device. With its unique internal architecture the digital core is optimized for low gate count and low latency applications. For efficient power management, the core can implement the Magic Packets detection. The MTIP_MAC1G is able to recover from SEU and to report any detected errors with the help of its embedded reliability features. Detected errors are then reported to external system and to internal sub-system. The MTIP_MAC1G matches major needs of any critical application and mainly those which require a DO-254 DAL-A compliance in the aerospace area.

The development has been done according to the RTCA/DO-254 ED-80 guidelines.

This component has been developed, verified and licensed by DMAP.

DELIVERABLES

- Verilog RTL sources code compliant with DMAP's design standard.
- SystemVerilog Functional verification test-benches using best-in class BFM from Mentor Graphics with full code and functional coverage.
- Reference Design as integration example (Dry Run) on Altera device.
- DMAP's support includes technical integration, DO-254 integration and certification phases.
- IP Datasheet and Customer Requirement Specification (CRS) document.

It includes all required data for RTCA/DO-254/ED-80 certification, including configuration management records, change management records and assurance process records:

- **Hardware Planning Process**: Hardware Development Plan (HDP), Hardware Validation and Verification Plan (HVVP), Hardware Configuration Management Plan (HCMP), Hardware Process Assurance Plan (HPAP) and Plan for Hardware Aspects of Certification (PHAC).
- **Standards**: Hardware Requirement Standard (HRS), Hardware Design Standard (HDS).
- **Hardware Development Process**: Hardware Requirement Document (HRD), Hardware Conceptual Document (HCD), Hardware Detailed Document (HDD), Hardware Traceability Matrixes (HTM), Hardware Accomplishment Summary (HAS) and Hardware Software Interface Document (HSID).
- **Hardware Verification and Validation Process**: Hardware Verification Cases Procedures (HVCP) and Hardware Verification Results (HVR) and validation activities reports.
- **Design Assurance Records:**
  - **Peer Reviews, Project Reviews**: Initial Design Review (IDR), Preliminary Design Review (PDR), Critical Design Review (CDR) and Final Design Review (FDR).
  - **Audits, Hardware Reviews:** Stage of Involvement (SOI) #1, #2, # 3 and #4.
- **Hardware Configuration Management Process**: Hardware Configuration Index (HCI), Hardware Environment Configuration Index (HECI).

CONTACT

For further product's information and other DMAP's services please contact:
Email: contact@dmap.fr
Web: http://www.dmap.fr
Phone: +33(0)4 42 61 29 13
100, Impasse des Houillères - 13590 Meyreuil - France.

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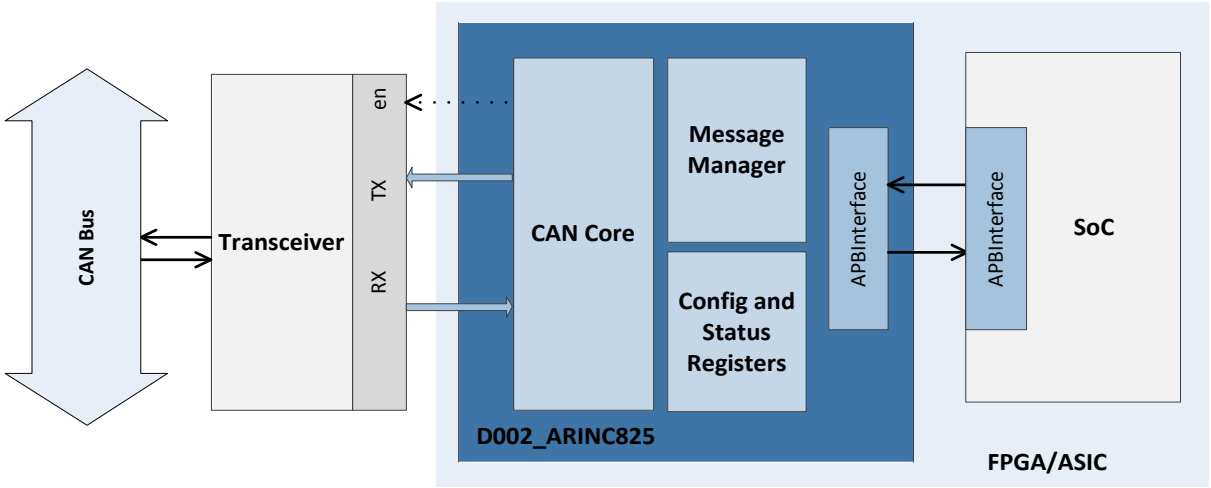
DO254-IP: D002_ARINC825

KEY FEATURES

- Developed according to DO-254/ED-80 guidance. Compliant DAL A.
- Compliant with ARINC825-1 Specification. May 10, 2010.
- Compliant with CAN 2.0 Specification (v 2.0) published by Bosh (part A and part B).
- Support Transceiver ISO1050 from Texas Instrument and Philips TJA1040 with Standby mode.



TECHNICAL FEATURES

- Bit rates up to 1 Mbits/s are possible at network length below 40 m.
- Supports 1Mbps, 500kbits, 250kbits, 125kbits and low speed at 83.33kbits with configurable baud rate generator.
- CAN 2.0 part A and B: base frame format (11 identifier bits) and extended frame format (29 identifier bits).
- CAN High speed: up to 30 nodes.
- Support TXD/RXD interface for external transceiver (TI ISO1050-SLL983C)
- Support 8/16/32-bits APB interface with separate clock domain.
- 64 byte receive Message FIFO
- Message filtering
- Normal and listen Only Mode
- Single shot transmission
- Local and Global self test
- Technology independent (Altera/Xilinx/Actel/ASIC).

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OVERVIEW

CAN is a message-based protocol, designed specifically for automotive applications but now also used in other areas such as avionics equipment in safety critical application. The CAN Interface module is a dedicated interface which enables data communication for ARINC825 application layer. It allows a system with an embedded CAN bus to transmit information quickly and surely. The hardware item only covers digital layers of the CAN Protocol bus architecture. The D002_ARINC825 matches major needs of any critical application and mainly those which require a DO-254 DAL-A compliance in the aerospace area.

The development has been done according to the RTCA/DO-254 ED-80 guidelines.

This component has been developed, verified and licensed by DMAP.

DELIVERABLES

- VHDL RTL sources code compliant with DMAP's design standard.
- VHDL verification test-benches with 100% code coverage and functional requirement coverage.
- Reference Design as integration example (Dry Run) on Xilinx® device.
- DMAP's support includes technical integration, DO-254 integration and certification phases.
- IP Datasheet and Customer Requirement Specification (CRS) document.

It includes all required data for DO-254/ED-80 certification, including configuration management records, change management records and assurance process records:

- **Hardware Planning Process**: Hardware Development Plan (HDP), Hardware Validation and Verification Plan (HVVP), Hardware Configuration Management Plan (HCMP), Hardware Process Assurance Plan (HPAP) and Plan for Hardware Aspects of Certification (PHAC).
- **Standards**: Hardware Requirement Standard (HRS), Hardware Design Standard (HDS).
- **Hardware Development Process**: Hardware Requirement Document (HRD), Hardware Conceptual Document (HCD), Hardware Detailed Document (HDD), Hardware Traceability Matrixes (HTM), Hardware Accomplishment Summary (HAS) and Hardware Software Interface Document (HSID).
- **Hardware Verification and Validation Process**: Hardware Verification Cases Procedures (HVCP) and Hardware Verification Results (HVR) and validation activities reports.
- **Design Assurance Records:**
  - **Peer Reviews.**
  - **Design Reviews**: Initial Design Review (IDR), Preliminary Design Review (PDR), Critical Design Review (CDR) and Final Design Review (FDR).
  - **Hardware Reviews:** Stage of Involvement (SOI) #1, #2, #3 and #4.
  - **Audits.**
- **Hardware Configuration Management Process**: Hardware Configuration Index (HCI), Hardware Environment Configuration Index (HECI).

CONTACT

For further product's information and other DMAP's services please contact:
Email: contact@dmap.fr
Web: http://www.dmap.fr
Phone: +33(0)4 42 61 29 13
100, Impasse des Houillères - 13590 Meyreuil - France.

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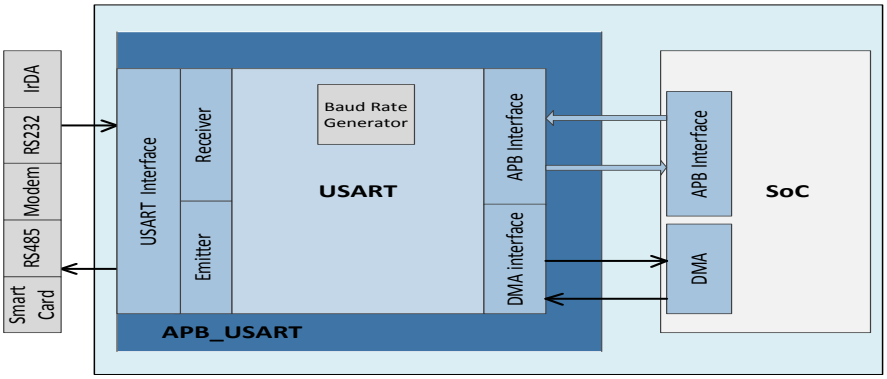
DO254-IP: APB/USART

KEY FEATURES

- Developed according to RTCA/DO-254 ED-80 guidance. Compliant DAL A.
- Universal Synchronous Asynchronous Receiver Transmitter.
- Interfaces on RS485 buses, ISO7816 smart card slots, infrared transceivers and modem ports.
- Compliant with AMBA 3 APB Protocol v1.0.



TECHNICAL FEATURES

- Programmable Baud Rate Generator
- Communication at up to 115.2 Kbps
- 5- to 9-bit Full-duplex Synchronous or Asynchronous Serial Communications
- MSB-first or LSB-first
- 1, 1.5 or 2 Stop Bits in Asynchronous Mode or 1 or 2 Stop Bits in Synchronous Mode
- Parity Generation and Error Detection
- Optional Break Generation and Detection
- By 8 or by 16 Over-sampling Receiver Frequency
- Optional Hardware Handshaking RTS-CTS
- Receiver Time-out and Transmitter Time guard
- Optional Modem Signal Management
- RS485 with Driver Control Signal
- ISO7816 protocols support
- IrDA Modulation and Demodulation
- Supports Connection of Two Direct Memory Access Channels (DMA)

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OVERVIEW

The Universal Synchronous Asynchronous Receiver Transceiver (USART) provides one full duplex universal synchronous asynchronous serial link. Data frame format is programmable (word length, parity, number of stop bits) to support a large number of standards. Receiver error detection is implemented (parity, framing, overrun detection). The APB_USART supports specific operating modes providing interfaces on RS485 buses, with ISO7816 smart card slots, infrared transceivers and connection to modem ports. The hardware handshaking feature enables an out-of-band flow control by automatic management of the pins RTS and CTS.

The APB_USART matches major needs of any critical application and mainly those which require a DO-254 DAL-A compliance in the aerospace area.

The development has been done according to the RTCA/DO-254 ED-80 guidelines.
This component has been developed, verified and licensed by DMAP.

DELIVERABLES

- Verilog RTL sources code compliant with DMAP's design standard.
- Functional verification test-benches using a BFM and a score board to compare final result.
- Reference Design as integration example (Dry Run) on FPGA device.
- DMAP's support includes technical integration, DO-254 integration and certification phases.
- IP Datasheet and Customer Requirement Specification (CRS) document.

It includes all required data for RTCA/DO-254/ED-80 certification, including configuration management records, change management records and assurance process records:

- **Hardware Planning Process**: Hardware Development Plan (HDP), Hardware Validation and Verification Plan (HVVP), Hardware Configuration Management Plan (HCMP), Hardware Process Assurance Plan (HPAP) and Plan for Hardware Aspects of Certification (PHAC).
- **Standards**: Hardware Requirement Standard (HRS), Hardware Design Standard (HDS).
- **Hardware Development Process**: Hardware Requirement Document (HRD), Hardware Conceptual Document (HCD), Hardware Detailed Document (HDD), Hardware Traceability Matrixes (HTM), Hardware Accomplishment Summary (HAS) and Hardware Software Interface Document (HSID).
- **Hardware Verification and Validation Process**: Hardware Verification Cases Procedures (HVCP) and Hardware Verification Results (HVR) and validation activities reports.
- **Design Assurance Records:**
  - **Peer Reviews, Project Reviews**: Initial Design Review (IDR), Preliminary Design Review (PDR), Critical Design Review (CDR) and Final Design Review (FDR).
  - **Audits, Hardware Reviews:** Stage of Involvement (SOI) #1, #2, # 3 and #4.
- **Hardware Configuration Management Process**: Hardware Configuration Index (HCI), Hardware Environment Configuration Index (HECI).

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Web: http://www.dmap.fr
Phone: +33(0)4 42 61 29 13
100, Impasse des Houillères – 13590 Meyreuil - France

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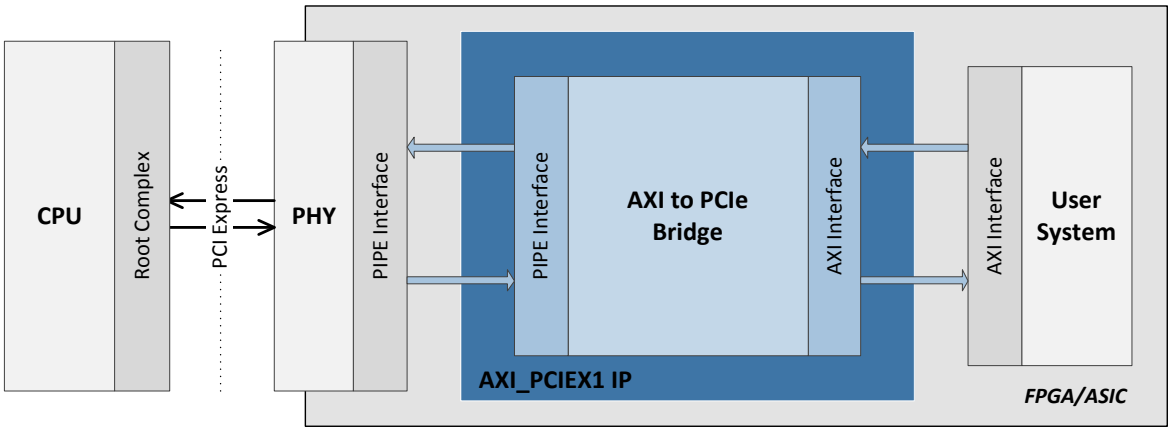
DO254-IP: PCI EXPRESS®

KEY FEATURES

- Developed according to RTCA/DO-254 ED-80 guidance. Compliant DAL A.
- Compliant with PCIe Specification 2.0 – Gen1.
- Compliant with AMBA AXI Protocol version 2.0.
- Compliant with PIPE version 1.0. PHY Interface for the PCI Express® Architecture.



TECHNICAL FEATURES

- PCI Express® Endpoint Gen 1 at 2.5 Gbps.
- One Lane (x1).
- PIPE: 16 bits interface (Optional 8 bits). PIPE Clock frequency is 250MHz in 8 bits or 125MHz in 16 bits.
- AMBA AXI4: 32 bits data/address Slave and Master Interfaces
- User interface for Configuration and Status Registers.
- Supports 6 BAR (Base Address Registers).
- Supports PCIe Power Management capability: ASPM L0s and L1.
- Optional MSI capabilities.
- Full AER capability implemented.
- Full report done to Root Complex and to user application. (Parity check on data buffers, FSM monitoring)
- Implements Advanced Reliability features for critical applications.
- Optimized for low gate count (4-5k LE on FPGA) and low core latency.
- Technology independent (Altera/Xilinx/Actel/ASIC).
- Configurable buffer size from 512B to 2kB depending on performance requirement.

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OVERVIEW

The AXI_PCIEX1 module is a PCI Express® to AXI Bridge. It allows a system with an embedded AXI bus to be connected to an external PCI Express® Bus. The hardware item only covers digital layers of the PCI Express® bus architecture. In a typical system the main external processor is able to address the internal AXI bus used to interconnect all internal components all together. With its unique internal architecture the digital core is optimized for low gate count and low latency applications. The AXI_PCIEX1 is able to recover from SEU and to report any detected errors with the help of its embedded reliability features. Detected errors are then reported to external processor and to internal sub-system. The AXI_PCIEX1 matches major needs of any critical application and mainly those which require a DO-254 DAL-A compliance in the aerospace area.

The development has been done according to the RTCA/DO-254 ED-80 guidelines.

This component has been developed, verified and licensed by DMAP.

DELIVERABLES

- Technology independent Verilog RTL sources code compliant with DMAP's design standard.
- SystemVerilog Functional verification test-benches using best-in class BFM from Mentor Graphics with full code and functional coverage.
- Reference Design as integration example (Dry Run) on Xilinx device.
- DMAP's support includes technical integration, DO-254 integration and certification phases.
- IP Datasheet and Customer Requirement Specification (CRS) document.

It includes all required data for RTCA/DO-254/ED-80 certification, including configuration management records, change management records and assurance process records:

- **Hardware Planning Process**: Hardware Development Plan (HDP), Hardware Validation and Verification Plan (HVVP), Hardware Configuration Management Plan (HCMP), Hardware Process Assurance Plan (HPAP) and Plan for Hardware Aspects of Certification (PHAC).
- **Standards**: Hardware Requirement Standard (HRS), Hardware Design Standard (HDS).
- **Hardware Development Process**: Hardware Requirement Document (HRD), Hardware Conceptual Document (HCD), Hardware Detailed Document (HDD), Hardware Traceability Matrixes (HTM), Hardware Accomplishment Summary (HAS) and Hardware Software Interface Document (HSID).
- **Hardware Verification and Validation Process**: Hardware Verification Cases Procedures (HVCP) and Hardware Verification Results (HVR) and validation activities reports.
- **Project Review**: Initial Design Review (IDR), Preliminary Design Review (PDR), Critical Design Review (CDR) and Final Design Review (FDR).
- **Hardware Configuration Management Process**: Hardware Configuration Index (HCI), Hardware Environment Configuration Index (HECI).

CONTACT

For further product's information and other DMAP's services please contact:
Email: contact@dmap.fr
Web: http://www.dmap.fr
Phone: +33(0)4 42 61 29 13
100, Impasse des Houillères – 13590 Meyreuil - France

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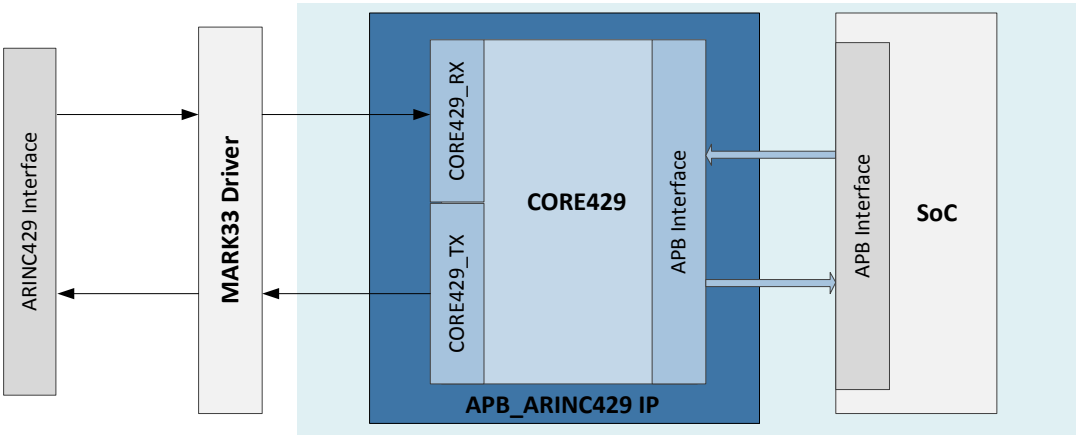
DO254-IP: ARINC429

KEY FEATURES

- Developed according to DO-254/ED-80 guidance. Compliant DAL A.
- Compliant with ARINC 429 Protocol published on September 27, 2001.
- Compliant with AMBA 3 APB Protocol v1.0.
- Compliant with Mark 33 Digital Information Transfer System.



TECHNICAL FEATURES

- Clock frequency configurable in 1 MHz, 10 MHz, 16 MHz or 20 MHz
- 512 bytes of APB address space
- Rx and Tx ARINC429 Channels number independently configurable from 1 to 16
- ARINC429 input and output configurable in Low (12.5 kHz or 50 kHz) or High (100 kHz) speed mode
- One FIFO for each ARINC429 channel
- ARINC429 channel FIFO depth configurable in 32, 64, 128, 256 or 512 bits
- APB_ARINC429 IP supports up to 256 unique labels per Receive channel
- AMBA APB Read data bus width and Write data bus width configurable in 8, 16 or 32 bits
- A support Source/Direction Identifiers mechanism per Receive channel
- A loopback mode for safety and testing purpose
- Supporting the main FPGA device families and can be fitted in an ASIC target

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OVERVIEW

The APB_ARINC429 module is an ARINC429 to APB Bridge. It allows a system with an embedded APB bus to be connected to an external ARINC429 interface. The hardware item only covers digital layers of the ARINC 429 Protocol bus architecture. With its unique internal architecture the digital core is optimized for low gate count and low latency applications. The APB_ARINC429 matches major needs of any critical application and mainly those which require a DO-254 DAL-A compliance in the aerospace area.

The development has been done according to the DO-254/ED-80 guidelines.
This component has been developed, verified and licensed by DMAP.

DELIVERABLES

- Verilog RTL sources code compliant with DMAP's design standard.
- Verilog verification test-benches using a BFM, a data and configuration generator, a CPU and a score board to compare final result.
- Reference Design as integration example (Dry Run) on Actel® device.
- DMAP's support includes technical integration, DO-254 integration and certification phases.
- IP Datasheet and Customer Requirement Specification (CRS) document.

It includes all required data for DO-254/ED-80 certification, including configuration management records, change management records and assurance process records:

- **Hardware Planning Process**: Hardware Development Plan (HDP), Hardware Validation and Verification Plan (HVVP), Hardware Configuration Management Plan (HCMP), Hardware Process Assurance Plan (HPAP) and Plan for Hardware Aspects of Certification (PHAC).
- **Standards**: Hardware Requirement Standard (HRS), Hardware Design Standard (HDS).
- **Hardware Development Process**: Hardware Requirement Document (HRD), Hardware Conceptual Document (HCD), Hardware Detailed Document (HDD), Hardware Traceability Matrixes (HTM), Hardware Accomplishment Summary (HAS) and Hardware Software Interface Document (HSID).
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