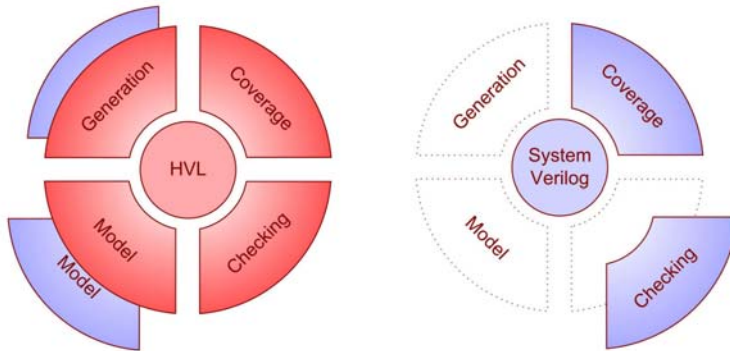


Mentor Consulting: Verification Language Migration Services

D A T A S H E E T



To realize the maximum value from a new verification methodology, legacy code and testbenches are preserved and migrated to the new environment.

Major Service Offerings

- Expert migration services
- Comprehensive testbench translation
- Proven, structured process
- Preserve legacy verification investments

Major Service Benefits

- Mentor Consulting provides an efficient and economic solution for completing the migration process
- Helps ease pressure of meeting development cycle deadlines

Unraveling the Verification Knot

Historically, ASIC design groups have used a wide variety of strategies in their attempt to unravel the verification knot. Technology forced them to create their own high level testbench solution. Languages varied, but the more successful groups adopted object-oriented programming (OOP) techniques. These languages offered the advantage of OOP's productivity and reuse features but introduced performance implications since they had to be used in co-simulation environments with established hardware simulators. The introduction and adoption of the SystemVerilog standard (IEEE-1800™) allows all groups to share one high level language throughout the entire design and verification process.

Migration: No Pain, No Gain

Verification is the fastest growing phase of the design process and everyone is seeking new and innovative ways to manage this growth. Meanwhile, competitive pressures continue to drive manufacturers to shorter development cycles and lower development costs.

SystemVerilog provides a single, standard language for both design and verification. This cuts the HDL/HVL workload by as much as one-half. A single language means only having to learn and work with one syntax and one design and verification tool. Mentor Graphics has taken this to the next level with its Questa™ verification platform, building upon the solid foundation established by the ModelSim simulator. The Questa single kernel implementation supports SystemVerilog as well as SystemC and PSL

Once the decision to move to SystemVerilog has been made, what about the substantial legacy investment in verification and testbenches that exists? To realize the maximum value of a new verification environment and methodology, this legacy must be preserved and migrated to the new environment. This is not a simple process and it diverts resources from their best use – designing products. But it is a necessary pain to realize the gain that SystemVerilog brings.

Migration Services: Ease the Pain, Enhance the Gain

Fortunately, migration is a once-and-done event. Therefore, developing in-house migration expertise is at best an unwise diversion and at worst a bad investment. Migration tasks can be easily and economically outsourced, freeing designers to work on product development.

At Mentor Consulting, migration services are a specialty. These services facilitate testbench migration from e or Vera® to SystemVerilog. Our consultants are fluent in all of these languages. They have developed a proven migration process and understand the concerns and tradeoffs associated with the migration activity. Our pragmatic approach ensures the migrated testbench represents as good an architecture as the original – or better.

A Proven Migration Process

Mentor Consulting's Verification Language Migration Services are designed to incrementally migrate sections of the legacy testbench. As each section is migrated, it is

carefully checked for accuracy before proceeding. All legacy metrics are preserved first and foremost throughout the process. This ensures complete confidence that the migrated testbench is as good as, or better than, the legacy version.

Coverage Migration

Functional coverage points give the best indication of a test's operation. Coverage points are migrated first and the legacy tests(s) are run. The coverage results, both from the legacy HVL and SystemVerilog, are compared to ensure they are identical. This step lays a solid foundation for the rest of the migration process as it migrates two key elements:

Type Migration

Any testbench types used in coverage groups are migrated to SystemVerilog as well as all other static types. This allows coverage data to be modeled identically in both languages.

Event Migration

Functional coverage metrics use these events to decide when to collect coverage. Any testbench events used in coverage collection are migrated to SystemVerilog as well as all events in the architecture. This migrates all the elements necessary for coverage collection.

Checking Migration

Data and temporal checks are next migrated into SystemVerilog. For this, the frameworks for automatic checking mechanisms such as bus monitors are migrated. These checks are then added. The legacy testbench is rerun and the checks, operating in parallel, are confirmed to behave identically. This allows an opportunity to analyze the completeness and effectiveness of the legacy checking. SystemVerilog adoption enables assertion-based verification (ABV), which automates check execution. More importantly, checks (assertions) are embedded in design modules where they detect faults closer to the root cause and execute at all levels of abstraction. This step includes the migration of the next major section of the legacy HVL code.

Class Migration

All object-oriented languages are collections of classes. The legacy classes are migrated to SystemVerilog classes identically. This is effectively the bulk of the testbench migration. As all the classes are migrated, the new SystemVerilog testbench takes shape.

Function Migration

Embedded in the classes are existing tasks or functions. These are migrated next. Building upon the events migrated earlier, all functions and tasks are migrated. The legacy tests are run again with the migrated architecture and confirmed to be cycle-accurate.

Model Migration

With the checking and coverage confirmed to operate, the legacy testbench support models are migrated. This includes any legacy HVL models. Confirming that this section has migrated requires that both testbenches operate identically when given the same input. To accomplish this, static stimulus data is used for the migrated testbench and the legacy testbench.

Generation Migration

With all the testbench sections fundamentally migrated and checked, the final step is to translate the random generation directives. This is a relatively simple, straightforward operation. At this point however, since there is no standard algorithm for random generation, the legacy HVL and SystemVerilog testbench stimulus will tend to diverge. Simulating with several random seeds should result in comparable coverage.

The legacy testbench, now migrated, is archived and future enhancements such as assertions, formal and unified coverage are added to the single kernel, single license, SystemVerilog testbench.

How Long Does Migration Take?

Because no two testbenches are the same, it is impossible to provide a generic guideline for the length of the overall translation process. However, Mentor Consulting can provide a quote for a translation project after a brief analysis of existing code.

About Mentor Consulting

Mentor Consulting provides customers with excellence and expertise in electronic design automation infrastructure and methodology. It is the only service partner in the industry that invests in the transfer of knowledge to its customers to ensure a smooth deployment and integration of new tools and methods. Mentor Consulting solutions for silicon yield enhancement, verification, cabling, and data management are engaged worldwide by forward-looking electronics companies to optimize design productivity and advance adoption of the latest industry design best practices. For more information, contact mentor_consulting@mentor.com or visit www.mentor.com/consulting.

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