



# **Questa® ADMS™ for A/MS Design Verification Student Workbook**

---

**© 1995-2012 Mentor Graphics Corporation  
All rights reserved.**

This document contains information that is trade secret and proprietary to Mentor Graphics Corporation or its licensors and is subject to license terms. No part of this document may be photocopied, reproduced, translated, distributed, disclosed or provided to third parties without the prior written consent of Mentor Graphics..

This document is for information and instruction purposes. Mentor Graphics reserves the right to make changes in specifications and other information contained in this publication without prior notice, and the reader should, in all cases, consult Mentor Graphics to determine whether any changes have been made.

The terms and conditions governing the sale and licensing of Mentor Graphics products are set forth in written agreements between Mentor Graphics and its customers. No representation or other affirmation of fact contained in this publication shall be deemed to be a warranty or give rise to any liability of Mentor Graphics whatsoever.

MENTOR GRAPHICS MAKES NO WARRANTY OF ANY KIND WITH REGARD TO THIS MATERIAL INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE.

MENTOR GRAPHICS SHALL NOT BE LIABLE FOR ANY INCIDENTAL, INDIRECT, SPECIAL, OR CONSEQUENTIAL DAMAGES WHATSOEVER (INCLUDING BUT NOT LIMITED TO LOST PROFITS) ARISING OUT OF OR RELATED TO THIS PUBLICATION OR THE INFORMATION CONTAINED IN IT, EVEN IF MENTOR GRAPHICS CORPORATION HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES.

#### **RESTRICTED RIGHTS LEGEND 03/97**

U.S. Government Restricted Rights. The SOFTWARE and documentation have been developed entirely at private expense and are commercial computer software provided with restricted rights. Use, duplication or disclosure by the U.S. Government or a U.S. Government subcontractor is subject to the restrictions set forth in the license agreement provided with the software pursuant to DFARS 227.7202-3(a) or as set forth in subparagraph (c)(1) and (2) of the Commercial Computer Software - Restricted Rights clause at FAR 52.227-19, as applicable.

**Contractor/manufacturer is:**

Mentor Graphics Corporation

8005 S.W. Boeckman Road, Wilsonville, Oregon 97070-7777.

Telephone: 503.685.7000

Toll-Free Telephone: 800.592.2210

Website: [www.mentor.com](http://www.mentor.com)

SupportNet: [supportnet.mentor.com/](http://supportnet.mentor.com/)

Send Feedback on Documentation: [supportnet.mentor.com/doc\\_feedback\\_form](http://supportnet.mentor.com/doc_feedback_form)

**TRADEMARKS:** The trademarks, logos and service marks ("Marks") used herein are the property of Mentor Graphics Corporation or other third parties. No one is permitted to use these Marks without the prior written consent of Mentor Graphics or the respective third-party owner. The use herein of a third-party Mark is not an attempt to indicate Mentor Graphics as a source of a product, but is intended to indicate a product from, or associated with, a particular third party. A current list of Mentor Graphics' trademarks may be viewed at: [www.mentor.com/trademarks](http://www.mentor.com/trademarks).

**End-User License Agreement:** You can print a copy of the End-User License Agreement from: [www.mentor.com/eula](http://www.mentor.com/eula).

# Table of Contents

---

## Module 1

<b>Introduction to Questa ADMS.....</b>	<b>9</b>
Objectives .....	9
Challenges of MS SOC Verification .....	10
Approaches to AMS Verification .....	11
Approach 1 : Keep it Digital ! .....	12
Approach 2 : Fast-SPICE.....	14
Approach 3 : VHDL-AMS / Verilog-AMS .....	16
Our Solution : Allow Flexibility .....	18
Comprehensive Technology .....	19
Digital-Centric Methodology.....	20
Analog-Centric Methodology .....	21
Flexible - Scalable Architecture .....	22
Questa ADMS Unified Platform for All Design Methodologies .....	23
In Either Major Integration....	24
Artist Link for Cadence ADE .....	25
Or Questa ADMS Standalone .....	26
A/MS Simulation Required Tasks .....	27
Questa ADMS Flow on an Example .....	28
Load Design Window .....	29
Questa ADMS Main Window .....	30
Selecting Signals/Nets for Viewing.....	31
Selecting Signals/Nets for Viewing Other Method .....	32
Running a Simulation .....	33
Viewing Results With EZwave: A True Mixed-Signal Waveform Viewer .....	34
EZwave: Elements of the Interface .....	35
EZwave: Additional Tools.....	36
EZwave Help .....	37
Other Useful Information.....	38
Lab Exercise – Lab 1 .....	39

## Module 2

<b>Library Management .....</b>	<b>41</b>
Objectives .....	41
What Is an ADMS Library?.....	42
Logical Library Names .....	43
Sample Initialization Files .....	44
Objectives .....	45
ADMS Library Management Commands: Overview .....	46
ADMS Library Management Commands: Library Creation.....	47
ADMS Library Management Commands: Change WORK .....	48
ADMS Library Management Commands: WORK Contents .....	49

Library Management Example .....	50
Commonly-Used Library Management Commands .....	52
Viewing Library Content in the GUI .....	53
Objectives .....	54
Populating Libraries: Compiling Models .....	55
Compilation Commands .....	56
QuestaSim Library Usage in Questa ADMS .....	57
Library Compatibility Management .....	58
Automatic Recompilation .....	59
VAMAKE .....	60
Lab Exercise – Lab 2 .....	61
<b>Module 3</b>	
<b>Basic Mixed-Signal Simulation .....</b>	<b>63</b>
Objectives .....	63
Questa ADMS Data Flow .....	64
Steps for Running Simulations .....	65
New GUI in AMS2009.1 .....	66
Questa ADMS GUI Settings .....	67
Structure Window: Unified Design View .....	68
Invoking the Questa ADMS Simulator .....	69
Command Line vasim .....	70
Command File .....	71
Additional vasim Examples .....	72
vasim: Other Commonly-Used Options .....	73
Statistics File .....	74
vasim –cmd ..... –g/-G To Override Value of Digital or Analog Parameters .....	75
vasim –G/-g .....	76
Objectives .....	77
Dofile .....	78
TCL Commands .....	79
How to Plot a Group of Nodes .....	80
In Case of Waveform Database Failure .....	81
Lab Exercise – Lab 3 .....	82
<b>Module 4</b>	
<b>Simulating Analog Centric Designs .....</b>	<b>83</b>
Objectives .....	83
Analog-Centric Methodology .....	84
Procedure for SPICE Instantiating HDL .....	85
.model and Y- instance Syntax .....	86
Generics in Y-instance .....	87
Replacing SPICE With HDL .....	88
Example: SPICE Instantiating HDL .....	89
.MODEL Extension .....	90
Usage Example .....	91
SPICE Compatibility Options for Other SPICE “Flavors” .....	92
Objectives .....	93

## Table of Contents

---

Reconfigure SPICE Design .....	94
.BIND Syntax .....	95
Wildcard in .BIND .....	96
.BIND Example .....	97
.BIND: Other Arguments .....	98
.BIND: Resolving Port Mismatch .....	99
vamatch .....	100
vamatch Example .....	101
vamatch: Other Arguments .....	103
Lab Exercise – Lab 4 .....	104

## Module 5

### Simulating Digital Centric Designs ..... 105

Objectives .....	105
HDL Instantiating SPICE – Typical Situation .....	106
Starting From a Questa Digital Simulation .....	107
Simulating the Digital Design With Questa ADMS .....	108
Replacing Digital With Spice .....	109
Simulating the MS Design With Questa ADMS .....	110
Access to Both Viewers in Questa ADMS .....	111
Objectives .....	112
How Can QuestaSim Instantiate SPICE? .....	113
vaspi Command Does the Job .....	114
vaspi Mechanism .....	115
vaspi Example .....	117
Verilog Testbench .....	118
VHDL Testbench .....	119
Objectives .....	120
vaspi - Interactive .....	121
Port-Mapping Options .....	122
Moving Pins/Ports .....	123
vaspi: Map by Name .....	124
vaspi: Map by Name Result .....	125
vaspi: Unconnected Pins .....	126
vaspi: Save Port Mapping .....	128
Port Association File .....	129
Objectives .....	130
vaspi Command Line .....	131
Port Mismatch Between QuestaSim and SPICE .....	132
vaspi Port-Mapping Options .....	133
Objectives .....	134
Running vaspi Within a Digital Library .....	135
Vaspi - The Design Unit is VHDL .....	136
Vaspi - The Design Unit is Verilog .....	137
Objectives .....	138
Vaspi Extensions .....	139
Vaspi – noarch .....	140
Vaspi –noarch -cktname .....	141

Vaspi –noarch -digname .....	142
Vaspi .....	143
Objectives .....	144
Compilation Commands .....	145
Instance Compilation .....	146
More About VHDL Compilation .....	147
Verilog-AMS Instantiating SPICE .....	148
Specific Rules .....	149
Lab Exercise – Lab 5 .....	150
<b>Module 6</b>	
<b>Boundary Elements .....</b>	<b>151</b>
Objectives .....	151
Intelligent Converter Insertion .....	152
Mixed Connections Need Boundary Elements .....	153
Bi-Directional Boundary Insertion .....	154
Boundary Insertion for “inout” .....	155
Tunneling .....	156
Objectives .....	157
Built-In Converters .....	158
Built-In Converter Insertion Procedure .....	159
Built-In Converters Types .....	160
std_logic D2A Equivalent Circuit .....	161
Impedance of std_logic D2A .....	162
Other std_logic D2A Parameters .....	163
std_vsrc (fast_std_logic) and std_supply .....	164
std_logic A2D .....	165
Supply Dependent Converters .....	166
VHDL-AMS Custom Boundary Model .....	168
User-Defined VHDL-AMS D2A Converter .....	169
Verilog-AMS Connect Rules .....	170
Connectrules Syntax .....	171
Objectives .....	172
Global Assignment .....	173
.defhook Specification .....	174
Power Domain .....	176
A Fragment of a .conv File .....	177
In .conv File for a Uni-Directional Net .....	178
In .conv File for a Bi-Directional Net .....	179
Required Three Steps .....	180
Lab Exercise – Lab 6 .....	181
<b>Module 7</b>	
<b>Advanced Simulation Features .....</b>	<b>183</b>
Objectives .....	183
Hierarchical Design Objects References .....	184
Hierarchy Path Separator .....	185
Spice .plot Command .....	186

## Table of Contents

---

DO-File Commands - Hierarchical Definitions . . . . .	187
Objectives . . . . .	188
Net Spy for Analog and Digital Objects . . . . .	189
Net Spy for Analog Objects . . . . .	191
Lab Exercise – Lab 7 . . . . .	193
Objectives . . . . .	194
Incremental Runs . . . . .	195
Saving Simulation State During DC or Transient . . . . .	196
Restoring a Saved Simulation State . . . . .	197
<b>Appendix A</b>	
<b>Solving an ADMS Problem . . . . .</b>	<b>199</b>
Objectives . . . . .	199
What Is the MGC Doc System? . . . . .	200
How to Access the MGC Doc System . . . . .	201
Objectives . . . . .	202
MGC Doc System – InfoHub . . . . .	203
From the InfoHub, You Can . . . . .	204
From the InfoHub, You Can Also . . . . .	205
InfoHub – Support & Training Tab . . . . .	206
InfoHub – System Admin Tab . . . . .	207
InfoHub – Search Scope . . . . .	208
HTML-Based Documentation . . . . .	209
HTML – Search Scoping . . . . .	212
HTML – Search Results List . . . . .	213
HTML – Global Index . . . . .	214
HTML – My Topics . . . . .	215
Objectives . . . . .	216
Mentor Graphics Support . . . . .	217
Your First Visit: Login or Signup . . . . .	218
Your First Visit: Choose Your Product . . . . .	219
Overview: All About Your Product . . . . .	220
Troubleshoot . . . . .	221
Open a Service Request: Step 1 . . . . .	222
Open a Service Request: Step 2 . . . . .	223
Search . . . . .	224
Advanced Search . . . . .	225
Objectives . . . . .	226
AMS Releases . . . . .	227
Stable ‘Production’ Branch . . . . .	228
‘Advanced’ Branch . . . . .	229
Benefits . . . . .	230
<b>Appendix B</b>	
<b>vasetinimode . . . . .</b>	<b>231</b>
Objectives . . . . .	231
vasetinimode . . . . .	232

---

**Appendix C**

<b>EZwave Major Features.....</b>	<b>237</b>
Objectives .....	237
Basic EZwave Features .....	238
Advanced EZwave Capabilities.....	239
EZwave: Elements of the Interface .....	240
Joint Waveform Database (JWDB) .....	241
Memory Shortage Detection .....	242
Out of Memory .....	243
.wdb and .swd Files .....	244
Invoke EZwave in Standalone Mode .....	245
EZwave Integration in Artist Link.....	246
How to Start EZwave in Artist Link .....	247
Objectives .....	248
Toolbar.....	249
Mouse Strokes .....	250
Find Button .....	251
The Find Capability for Plotted Waveforms .....	252
Waveform List.....	253
EZwave - Additional Tools .....	254
Objectives .....	255
Measurement Tool.....	256
Objectives .....	258
Waveform Calculator.....	259
Using the Waveform Calculator .....	260
Objectives .....	263
Waveform Compare Tool .....	264
Waveform Compare Wizard .....	265
Comparison Method Selection.....	266
Viewing Waveform Comparison Results .....	267
Objectives .....	268
File > Save Menu.....	269
Tel File Example .....	270
Getting Help.....	271